REMARKS/ARGUMENTS

In the Office Action mailed January 18, 2008, claims 1-12 were rejected. In response, Applicants hereby request reconsideration of the application in view of the proposed claim amendments and the below-provided remarks. No claims are added or canceled.

For reference, proposed amendments are presented for claims 1 and 10. In particular, the proposed amendments for each of claims 1 and 10 clarify the direct connection of the first interface to the memory bus. These amendments are supported, for example, by the illustration of Fig. 1, as well as the subject matter of the accompanying description. Applicants respectfully request that the amendments be entered to put the claims in condition for allowance or to put the claims in better condition for appeal.

Claim Rejections under 35 U.S.C. 102

Claims 1, 6-15, 17-21, and 25-30 were rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. Pat. Pub. No. 2002/0116565, hereinafter Wang). However, Applicants respectfully submit that these claims are patentable over Wang for the reasons provided below.

Independent Claim 1

Claim 1 recites "a first interface for direct connection to a memory bus which connects the host microprocessor and the system memory, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

In contrast, Wang does not disclose an interface of the host controller for direct connection to a memory bus. Rather, Wang merely describes a host processor bus 31 which connects the host controller system 100 and, in particular, the host controller logic unit 22 directly to the host microprocessor 24. Wang, Fig. 1A. Although the host microprocessor is separately connected to the system memory 32 via another bus (see the bus between the host microprocessor 24 and the system memory 32 of Fig. 1A), the host processor bus does not directly connect the host controller system or the host controller logic unit to the memory bus between the host microprocessor and the system memory.

In other words, none of the interfaces shown or described by Wang provides a direct connection from the host controller system or the host controller logic unit to the memory bus between the host microprocessor and the system memory. The only connection between the host controller system and the system memory is an indirect connection through the host processor bus, which is connected to the host microprocessor. Since Wang does not disclose a direct connection from the host controller system and the host controller logic to the memory bus between the host microcontroller and the system memory, Wang also fails to disclose an interface of the host controller system for direct connection to the memory bus between the host microprocessor and the system memory. Therefore, Wang does not disclose all of the limitations of the claim because Wang does not disclose an interface for direct connection to the memory bus which connects the host microprocessor and the system memory. Accordingly, Applicants respectfully submit that claim 1 is patentable over Wang because Wang does not disclose all of the limitations of the claim.

Independent Claim 10

Applicants respectfully assert independent claim 10 is also patentable over Wang at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 10 recites "a memory bus, which connects the host microprocessor and the system memory" and a host controller comprising "a first interface for direct connection to the memory bus, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

Here, although the language of claim 10 differs from the language of claim 1 and the scope of claim 10 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 10. Accordingly, Applicants respectfully assert claim 10 is patentable over Wang because Wang does not disclose an interface for direct connection to a memory bus which connects the host microprocessor and the system memory.

Dependent Claims 2-9, 11, and 12

Claims 2-9, 11, and 12 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 10. Applicants respectfully assert claims 2-9, 11, and 12 are allowable based on allowable base claims. Additionally, each of claims 2-9, 11, and 12 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the proposed amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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